LAB – 2 (practice questions)

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1.

andgate.v

module andgate(

input a,

input b,

output y

);

assign y = a & b;

endmodule

andgate\_tb.v

module andgate\_tb();

reg a;

reg b;

wire y;

andgate iandgate(a, b, y);

initial

begin

$monitor("a=%b, b=%b,y=%b",a,b,y);

$dumpfile("and.vcd");

$dumpvars(0,andgate\_tb);

a = 0;b = 0;#10;

a = 0;b = 1;#10;

a = 1;b = 0;#10;

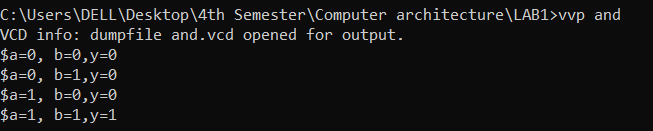
a = 1;b = 1;#10;

$finish;

end

endmodule

Screenshot:



2.

orgate.v

module orgate(

input a,

input b,

output y

);

assign y = a | b;

endmodule

orgate\_tb.v

module orgate\_tb();

reg a;

reg b;

wire y;

orgate iorgate(a, b, y);

initial

begin

$monitor("a=%b,b=%b,y=%b",a, b, y);

$dumpfile("or.vcd");

$dumpvars(0,orgate\_tb);

a = 0;b = 0;#10;

a = 0;b = 1;#10;

a = 1;b = 0;#10;

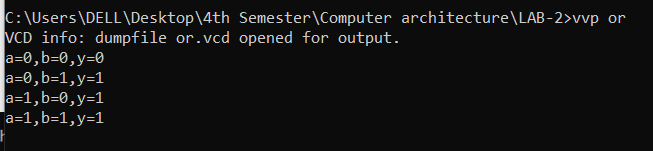
a = 1;b = 1;#10;

$finish;

end

endmodule

Screenshot:



3.

Notgate.v

module notgate(

input a,

output y

);

assign y = ~a;

endmodule

notgate\_tb.v

module notgate\_tb();

reg a;

wire y;

notgate inotgate(a,y);

initial

begin

$monitor("a=%b,y=%b",a,y);

$dumpfile("not.vcd");

$dumpvars(0,notgate\_tb);

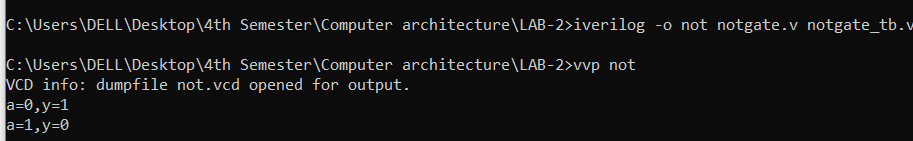
a = 0;#10;

a = 1;#10;

end

endmodule

screenshot:



4.

nandgate.v

module nandgate(

input a,

input b,

output y

);

assign y = ~(a & b);

endmodule

nandgate\_tb.v

module nandgate\_tb();

reg a;

reg b;

wire y;

nandgate verifynand(a,b,y);

initial

begin

$monitor("a=%b,b=%b,y=%b",a,b,y);

$dumpfile("nand.vcd");

$dumpvars(0,nandgate\_tb);

a = 0;b = 0;#10;

a = 0;b = 1;#10;

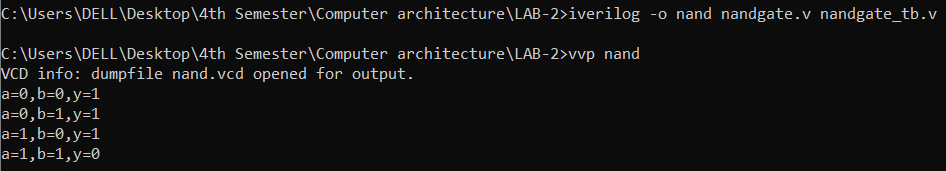
a = 1;b = 0;#10;

a = 1;b = 1;#10;

end

endmodule

screenshot:



5.

Norgate.v

module norgate(

input a,

input b,

output y

);

assign y = ~(a | b);

endmodule

norgate\_tb.v

module norgate\_tb();

reg a;

reg b;

wire y;

norgate verifynand(a,b,y);

initial

begin

$monitor("a=%b,b=%b,y=%b",a,b,y);

$dumpfile("norgate.vcd");

$dumpvars(0,norgate\_tb);

a = 0;b = 0;#10;

a = 0;b = 1;#10;

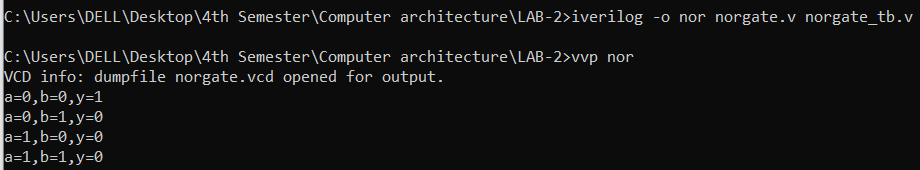
a = 1;b = 0;#10;

a = 1;b = 1;#10;

end

endmodule

screenshot:



6.

xorgate.v

module xorgate(

input a,

input b,

output y

);

xor x1(y,a,b);

endmodule

xorgate\_tb.v

module xorgate\_tb();

reg a;

reg b;

wire y;

xorgate verify(a,b,y);

initial

begin

$monitor("a=%b,b=%b,y=%b",a,b,y);

$dumpfile("xor.vcd");

$dumpvars(0,xorgate\_tb);

a = 0;b = 0;

a = 0;b = 1;

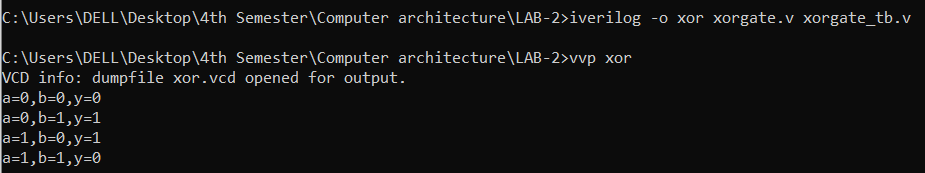
a = 1;b = 0;

a = 1;b = 1;

end

endmodule

screenshot:



7.

Xnorgate.v

module xnorgate(

input a,

input b,

output y

);

xnor x1(y,a,b);

endmodule

xnorgate\_tb.v

module xnorgate\_tb();

reg a;

reg b;

wire y;

xnorgate verify(a,b,y);

initial

begin

$monitor("a=%b,b=%b,y=%b",a,b,y);

$dumpfile("xnor.vcd");

$dumpvars(0,xnorgate\_tb);

a = 0;b = 0;#10;

a = 0;b = 1;#10;

a = 1;b = 0;#10;

a = 1;b = 1;#10;

end

endmodule

screenshot:

